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IN THE CLAIMS

What is claimed is:

1. A semiconductor device, comprising:  
2      a trench element separation region including a trench formed in a  
3      surface of a semiconductor substrate, the trench element separation region  
4      isolating separate semiconductor elements;  
5      an oxide film formed on inner walls of the trench;  
6      a trench filling insulating material filling the trench and having edges  
7      above the inner walls of the trench; and  
8      wherein a top section of the trench and the edges of the trench filling  
9      insulating material are formed so as to be essentially located on the same  
10     plane.

1. 2. The semiconductor device of claim 1, wherein the edges of the trench filling  
2      insulating material are defined by side edges of a sacrificial layer.

1. 3. The semiconductor device of claim 2, wherein the sacrificial layer is a silicon nitride  
2      film.

1. 4. The semiconductor device of claim 3, wherein:  
2      the side edges of the sacrificial layer are formed by an etching process  
3      including a neutral radical.

*SUB* 1 5. The semiconductor device of claim 1, wherein the semiconductor elements are  
2 insulated gate field effect transistors (IGFETs).

1 6. The semiconductor device of claim 5, wherein the IGFETs include opposite  
2 conductivity types.

*mult 3* 7. A semiconductor device, comprising:  
1 a trench element separation region including a trench formed in a  
2 surface of a semiconductor substrate, the trench element separation region  
3 isolating a first doped channel layer of a first insulated gate field effect  
4 transistor (IGFET) from a second doped channel layer of a second IGFET;  
5 an oxide film formed on inner walls of the trench;  
6 a trench filling insulating material filling the trench and having edges  
7 above the inner walls of the trench; and  
8 wherein inner wall edges in a top section of the trench and the edges of  
9 the trench filling insulating material are formed so as to be essentially located  
10 on the same plane.  
11

1 8. The semiconductor device of claim 7, wherein the edges of the trench filling  
2 insulating material are defined by side edges of a sacrificial layer.

*mult 4* 9. The semiconductor device of claim 8, wherein:

2 the side edges of the sacrificial layer are formed by an etching process  
3 including a fluorine radical.

1 10. The semiconductor device of claim 7, wherein the first and second doped channel  
2 layers are of the same conductivity types.

1 11. The semiconductor device of claim 7, wherein the first and second doped channel  
2 layers are of opposite conductivity types.

1 12. A method for forming a trench element separation region on a surface of a  
2 semiconductor substrate, comprising the steps of:

3 depositing a first insulation film onto the surface of the semiconductor  
4 substrate;

5 depositing and patterning a second insulation film to form a second  
6 insulation film pattern;

7 dry etching the semiconductor substrate using the second insulation  
8 film pattern as an etching mask to form a trench;

9 forming an oxide film on an inner wall of the trench by thermally  
10 oxidizing the semiconductor substrate using the second insulation film pattern  
11 as an oxidation mask;

12 removing a modified layer formed on the surface of the second  
13 insulation film during the thermal oxidation step by using a neutral radical  
14 including fluorine;

15 etching the surface of the second insulation film by a predetermined  
16 thickness after the modified layer is removed;  
17 depositing a filling insulation film over the whole surface of the trench  
18 to completely fill the trench after the surface of the second insulation film is  
19 etched; and  
20 chemically mechanical polishing the filling insulation film using the  
21 second insulation film as a polishing stopper to form a trench filling insulating  
22 material.

*Sub C*

1 13. The method for manufacturing a semiconductor device according to claim 12,  
2 wherein:

3 the second insulation film includes a silicon nitride film.

1 14. The method for manufacturing a semiconductor device according to claim 12,  
2 wherein:

3 the semiconductor substrate is a silicon substrate and the neutral  
4 radical is a fluorine radical.

1 15. The method for manufacturing a semiconductor device according to claim 14,  
2 wherein:

3 a final judgment of the modified layer removal is performed by  
4 measuring a change in intensity of emissions with a wavelength of  
5 approximately 336 nm from a reaction product NH.

1   **16.**   The method for manufacturing a semiconductor device according to claim 14,  
2   wherein:

3                     a final judgment of the modified layer removal is performed by  
4                     measuring a change in intensity of emissions with a wavelength of  
5                     approximately 388 nm from a reaction product CN.  
*Sub C*

1   **17.**   The method for manufacturing a semiconductor device according to claim 14,  
2   wherein:

3                     the thickness of the second insulation film is etched for adjustment  
4                     such that edges of the trench insulating material above the inner walls of the  
5                     trench are essentially located on the same plane as edges of the inner walls of  
6                     the trench in a top section of the trench.  
*ED*

1   **18.**   The method for manufacturing a semiconductor device according to claim 14, further  
2   including the step of:

3                     forming a doped channel layer of an insulated gate field effect  
4                     transistor (IGFET) by ion implantation and heat treatment after the trench  
5                     filling insulating material is formed.

1   **19.**   The method for manufacturing a semiconductor device according to claim 14,  
2   wherein:

3                     the first insulation film is a silicon oxide film formed by thermal

4                   oxidation of the semiconductor substrate; and  
5                   the filling insulation film is a silicon oxide film deposited by a vapor  
6                   deposition method.

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- 1       **20.** The method for manufacturing a semiconductor device according to claim 14,  
2           wherein:  
3                   the trench element separation region isolates a first insulated gate field  
4                   effect transistor (IGFET) from a second IGFET.

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